International Workshop on Nitride Semiconductors 2022

Conference report

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Introduction

The International Workshop on Nitride Semiconductors (IWN) series conference can be traced back to September 24-27, 2000, Nagoya international workshop on nitride semiconductors, which marks the first IWN. It is now the one of the largest events for nitride-based semiconductors. The IWN 2022 conference was held in Berlin, Germany, from 09 to 14 October.

This year, there were 813 participants from 32 countries. Germany, Japan, and the United States accounted for the top three by country of origin, with 217, 127, and 83 participants, respectively. The United Kingdom was ranked 7 with 33 participants. The program includes 67 invited presentations, 251 contributed talks, and 416 poster presentations, and was divided into four main sessions: (1) novel materials and nanostructures, (2) electronic and optical devices, (3) growth, and (4) characterization and optical characterization. Since my research focuses on GaN-based transistors, the majority of the talks I went to were in the field of electronics and I've highlighted them below.

Selected Presentations

Deep UV laser diode as an example of overcoming the semiconductor limit

- Hiroshi Amano, Nagoya University, JP.

AlGaN-based light-emitting devices (LEDs) were utilized to achieve deep ultraviolet (UV) emission at the UV-C (210 nm) region. However, in traditional impurity-controlled doping techniques, the higher activation energies of Mg for p-type AlGaN

and Si for n-type AlGaN are one of the challenges in the pursuit of improved light extraction efficiency and driving efficiency.

In this talk, Hiroshi introduced the concept of the distributed polarization doping (DPD) techniques which utilizes the strong polarization of AlGaN materials system, as an alternative method to overcome the limitations of impurity-controlled doping. Intentionally dopant-free p-n junctions formed by DPD were experimentally demonstrated. Non-impurity-doped p&n – $Al_xGa_{1-x}N$ with a graded Al mole fraction (x) was used. The DPD layers were designed to be perfectly strained on the GaN substrate, with the maximum Al mole fraction value of 13.2%, and grading widths up to 200 nm where cracking and lattice relaxation do not occur. SIMS data indicates a low Mg and Si profile of $< 5\times10^{16}$ cm^{-3} and 4×10^{15} cm^{-3} respectively. Built-in potential of > 3.37 V was extracted from C-V measurements and the space-charge concentration determined from C-V was higher than $> 5\times10^{17}$ cm^{-3}. It appears from the results that p-n junctions can be generated using DPD, and that these junctions can be employed in the same manner as those formed using traditional impurity doping. This method enables a path for the GaN-based electronics to eliminate the device limitations associated with conventional impurity doping.

High temperature performance of AIN MESFETs

- Masanobu Hiroki, NTT Basic Research Labs, JP.

Due to the large breakdown field of AIN (11-15 MV/cm), the AlN-based devices are attractive to obtain a smaller Ron compare with than GaN. It also suitable for the fusion, aerospace, and automobile applications due to the radiation hardness and high temperature tolerance. This talk demonstrates the AlN metal semiconductor field effect transistors (MESFETs) on SiC substrates with n-type AlN layer (Si : 2×10^{18} cm^{-3}) for the channel conduction and graded AlGaN layer (Si doped) for facilitate the n-type ohmic contact.

The device was characterized from the room temperature (RT) up to 500 ℃. At RT, the On-state drain current (I_d) was 420 μA/mm and the gate leakage current was < 10 fA/mm. The breakdown voltage was 1.7 kV at V_{gs} = - 20 V conditions with L_{gd} = 16 μm. With the increase the temperature, an increased drain current was observed. At 500 ℃, the On-state I_d was increased to 42 mA/mm and the OFF-state current was in

the range of 10^{-8} A/mm. The transconductance was also increased from 0.05 mS/mm to 4.5 mS/mm. The current ON/OFF ration of ~ 10^6 was achieved at 500 ℃. The increased I_d with temperature was attributed to increased electron concentration in the channel because of large ionization energy (250-280 meV) of Si. The buffer leakage current was attributed to the thermal activation of deep trap/donor states with activation energy of 0.61 eV and 0.97 eV by fitting of Arrhenius plot. These findings suggest that AlN MESFETs could be useful in high-voltage electronic devices that operate at high temperatures.

Design and characterization of p-body layer of vertical GaN devices on engineered substrates

-Matteo Borga, Interuniversity Microelectronics Centre, BE.

In this presentation, IMEC introduces its study of vertical GaN devices on the GaN-on-QST®. The QST® is an engineered coefficient of thermal expansion (CTE)-matched substrate with a poly AlN core and it is a CMOS fab-friendly 200 mm wafers. It also demonstrated an epitaxial growth of GaN buffer layers qualified for 1200 V applications on 200 mm QST® with a hard breakdown exceeding 1800 V.

For the vertical devices, the epitaxial structure with a 0.25 μm n^+-GaN layer for the bottom drain contact, a 3 μm lightly doped n^--GaN drift layer (Si: 4×10^{16} cm^{-3}), a 400 nm p-GaN (Mg doped) current blocking layer (CBL) and n^+-GaN layer for top source contact. For the drift region thickness, it can be grown up to > 10 μm without cracking. A 500~ 700V current blocking capability is achieved with 5 μm drift region thickness from diode structures. The 3-terminal device was a standard vertical trench MOSFET with inversion vertical sidewall MOS channel. The channel mobility was studies with varying Mg doping concentrations. An optimized inversion channel mobility of 43.48 cm^2/Vs was achieved with a Mg doping concentration of ~ 1×10^{19} cm^{-3}. A lower Mg doping concentration could achieve a higher inversion channel mobility close to ~ 100 cm^2/Vs, but with an expensed of higher off-state leakage. A higher Mg doping concentration on the other hand would result in the lower inversion mobility due to the impurity scattering. The findings of this study pave the way for the investigation of vertical GaN device development on a CMOS fab compatible substrate.

First demonstration of N-polar AlGaN/AlGaN high electron mobility transistor

-Srabanti Chowdhury, Stanford University, US.

In this talk, a N-polar AlGaN/AlGaN high electron mobility transistor (HEMT) concept was explored. The wafer epitaxy structure is as follows: $Al_xGa_{1-x}N/AlN/Al_yGa_{1-y}N/Al_{0.15}Ga_{0.85}N$ (25/2/25/600 nm) on sapphire substrate and it was grown by the MOCVD method. Top $Al_xGa_{1-x}N/AlN$ is to induce 2DEG for the channel conduction and $Al_yGa_{1-y}N$ serves as back barrier for a better 2DEG confinement. Mobility was measured close to 200 cm^2V/s and sheet carrier concentration of 2.46×10^{13} cm^{-2} at 0.2 Al mole fraction and the mobility shows a decreasing with increasing Al mole fraction (up to 80% Al mole fraction).

The 3-terminal device was then fabricated and characterized. The device parameters are W = 100 μm, L_g = 2 μm, L_{gs} = 4 μm and L_{gd} = 4 μm. The sheet resistance was 707 Ω/sq and contact resistance was 1.056 Ω.mm for a Ti/Al/Ni/Au metal scheme. For the output characteristics, device exhibits D-mode operation with a threshold voltage of ~ -16 V and current ON/OFF ratio of 10^8. A 250 mA/mm maximum drain current at V_{gs} = 0 V, V_{ds} = 13 V was measured. The current was 5 times higher than the previous demonstrated Ga polar AlGaN/AlGaN HEMT. Buffer breakdown was then characterized with over 1400V breakdown voltage for 10 μm spacing. This work demonstrates the potential of N-polar AlGaN/AlGaN architecture for the future high power and high frequency electronics applications.

Realization of low specific contact resistance on N-polar GaN surface using highly-doped n-type GaN film deposited by low-temperature reactive sputtering

- Shinji Yamada, Nagoya University, JP

As the emerging architecture of vertical GaN transistor on the bulk GaN substrate for high voltage applications, a backside contact with low resistance is essentially desired. In this talk, the low-temperature ohmic contact formation on the N-polar GaN surface by sputtering n^+-GaN methods was discussed. The low temperature ohmic contact

formation techniques provide additional advantageous to not affect the front-end device structures.

The sample was prepared by polishing the backside of the GaN substrates and deposition of 100 nm GaN (Si doped) on the polished surface by a reactive sputtering method. The Si and Ga target ratio was changed from 0 to 0.16 under constant Ga power conditions and the deposition temperature was compared between 500 ℃ and 600 ℃. The ohmic metallisation scheme was Ti/Al metal stacks and sintering at 475℃ for 5 min in N_2 environment for an ohmic contact formations. The hall measurement and circular transmission lime measurements were used to extract the sheet resistance (R_{sh}), mobility, and the specific contact resistance (ρ_c). It was observed that the increasing of Si/Ga ratio, the R_{sh} and ρ_c reduces. At the deposition conditions of 600 ℃ and Si/Ga ratio of 0.11, a high carrier concentration of 1.1×10^{20} cm^{-3} and mobility of 41.5 $cm^2/V.s$ were achieved with ρ_c of 1.5×10^{-5} Ωcm^{-3}. For the deposition temperature of 500 ℃ and Si/Ga ratio of 0.11, the mobility is slightly lower with a value of 17.5 $cm^2/V.s$ but the ρ_c is lower compared with 600 ℃ and the value of 1.1×10^{-5} Ωcm^{-3} is achieved. This talk highlights a low-temperature ohmic contact formations methods on the polished N-polar GaN surface and can be integrated into the future GaN device ohmic contact optimization.

Rump Session: What do we need to do to make III-nitrides surpass SiC in power electronics?

Professor Ramon Collazo, North Carolina State University, Prof. Dr. William Alan Doolittle, Georgia Institute of Technology, Dr. Andrew A. Allerman, Sandia National Laboratories, Professor Matteo Meneghini ,university of Padova, Dr Tetsuo Narita, Toyota Central R&D labs, and Dr Travis Anderson, the U.S. Naval Research Laboratory.

In this rump session, a discussion was held by the panel with other experts in the III-nitride community as audience. It began with a general introduction of each panel member's recent works/opinions and highlight the potential of III-nitrides. And then several key questions were asked.

It started with the discussion of bulk GaN wafer with the questions such as: can the technology provide for device requirement? -insulating/N-type/ wafer? Can the wafer diameter barrier be overcome? Can the costs requirement be met? The panel was generally agreed on the opinion that for GaN to compete SIC. 6 inch bulk GaN substrate

is needed in the future and the cost needed to be reduced in the range of serval hundreds euros. However, it is not available yet. More fundings/investment would be needed for the development of GaN substrate growth. It was also pointed out that GaN-on-foreign substrates is also a relatively acceptable candidate for the development of GaN electronics when the cost is a concern.

The second question raised was about the GaN doping. Can we achieve the needed doping in either GaN, AlGaN, or AlN?-Low or high doping? Is useful p-type doping possible and how? Do we have methods available to address thick layers with controllable doping? -HVPE, MOCVD or? What are the limitations in ion implantation of practice of type ion implantation?

For the growth methods, it was suggested that rapid MBE method could be used, and it doesn't need many effusion cells for growth GaN. On the other hand, Japanese researchers also suggested that they have demonstrated with >100 um GaN thickness with HVPE methods. For the ion implantation, it was pointed out that the main challenge is the change of Mg diffusion profile after the high temperature annealing. It was agreed that to adapt laser annealing techniques might be a way to better control the Mg diffusion issue.

The third part was about the device's architecture. What device architectural advantages can the III-nitride provide? What are the most convenient and advantageous approaches for vertical GaN? Which practical devices could be realized in AlGaN and AlN?- Is this technology feasible at all? For the device architecture point of view, one of the panel members suggest that we needed to be open mind to not only look back to the demonstrated architecture (lateral or vertical), the ultimate structures are not demonstrated yet. New ideas and concept would be needed for the future device architecture developments.

It was concluded by the most senior panel member that despite theoretical material merits of novel III-nitrides devices, or novel architectures, in the end, the device performances were limited by the passivation. When design/fabricate the devices, one needs to be very careful with the passivation. The most used passivation method is SIN passivation. Depending on the passivation conditions, it could be silicon related trap or nitrogen related trap. And these traps change the surface potential, consequently, the device performance could be very different.

Conclusion

I'd like to express my sincere thanks to the UK Nitrides Consortium, whose funding made it possible for me to present my research at this year's IWN and attend the conference in person to learn more about the fascinating work being conducted in the field of nitrides across the world.

By attending this conference, I have not only been able to learn the latest advances in the field of group III-nitride, but also have a chance discuss with the researchers from other institution around the word regarding the specific topic that interested me, such as the p-type doping and p-type ohmic contact's impacts on the body effect of vertical GaN transistors and learn from their opinions. Moreover, after presenting my work, I received positive feedback from topical experts and opens some new thoughts in my mind.