International Workshop on Nitride Semiconductors (IWN 2016)

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Introduction

The 2016 International Workshop on Nitride Semiconductors (IWN 2016) conference is held in Orlando, Florida, from 2nd to 7th October. The conference is one of the largest events for nitride based semiconductors. This year, it features 6 plenary talks, 64 invited talk, over 200 contributed oral presentations and approximately 500 poster presentations. The whole program is divided into 6 sessions including Fundamentals of Material Growth, Optical Devices, Electronic Devices, Basic Material Properties, Nanostructures and Novel Materials and Devices. As I am working on GaN based power transistors, most of the presentations I attended belongs to Electronic Devices, which is divided into two sub-sessions: RF/mm Wave Devices and Power Devices. Here, I will highlight some of the presentations that I found particularly interesting.

Selected Presentations

Umesh Mishra (USCB) – Current Status and Future Directions in GaN-Based Electronics (Plenary Talk)

Current status of GaN devices was summarized first. Tremendous efforts have been made on the development of the GaN RF and power devices. 650 V GaN devices were well demonstrated by companies such as Transphorm, GaN systems and Panasonic and were commercially available from Transphorm. The reliability and lifetime of the devices were also tested by JEDEC qualification that normally used on Si devices, by Transphorm.

Two new areas were then highlighted. First was the N-polar GaN based HEMTs. The major advantage of using N-polar GaN was the potentially high f_T and therefore the RF device could achieve a higher power density. The advantage was originated from the fact that the 2DEG is provided by the back barrier, which gives a better aspect ratio and enables the gate to be able to further scale down without the worry of short channel effect. The thinner GaN barrier compared to the AlGaN barrier in traditional Ga Polar structures also contributed to a higher g_m. Devices with an output power density of 6.7 W/mm (improving from around 2 W/mm in conventional Ga Polar devices) at 94 GHz was demonstrated. In addition, gate leakage was suppressed by a 2.6 nm AlGaN layer on top of the 20 nm GaN barrier, plus a SiNx gate dielectric. A GaN cap can effectively increase the channel mobility and

enables N-Polar device to compete with Ga-Polar ones. The N-Polar device was suggested for RF amplification and communication above 18GHz. Second was the Hot Electron Transistors (HETs). HETs utilised the electron scattering properties to achieve a device that is suitable for ultra-high frequency applications. By using a proper heterostructure, hot electrons can be injected from a higher energy hand area, but collected by a lower energy band area without physical intermedia. HETs may further push the performance limit of GaN HEMTs.

Dong Ji (Arizona State University) – Demonstration of Normally off GaN Trench-CAVET for High Power Application (Oral Presentation)

With the increase in the mobility of bulk GaN, GaN vertical structures now attract much more attentions for high power applications. This talk demonstrated the fabrication and DC characterisation of a GaN current aperture vertical electron transistor (CAVET).

The epitaxial structure with a 1 µm n-GaN layer, a 6 µm lightly doped n-GaN drift layer ($\sim 1e^{16}$ cm^{-3}) and a 400 nm p-GaN (Mg: $5e^{19}$ cm^{-3}) current blocking layer (CBL) was grown on a n-GaN free-standing substrate (Furukawa) by MOCVD. After ICP etching to form the aperture, a MOCVD regrowth was conducted to form a standard GaN HEMT structure on the top with a 140 nm UID GaN layer, a 25 nm AlGaN layer and a 30 nm SiNx passivation layer. The author claimed that the Mg diffusion problem during regrown can be controlled by the low temperature. In addition, the potential Si residual during regrown was cleaned by proper cleaning steps. The buried p-GaN was activated during the fabrication by subsequent annealing in Nitrogen at 700 °C.

The fabricated device exhibited a V_{th} of +20 V and a maximum output current of 100 A/cm^2. The output current can be further improved with implanted contacts. A breakdown voltage of the 225 V was achieved with a trench length of 2 µm. It was mainly a gate-drain breakdown which was claimed caused by the defects in the trench as the regrowth was on a non-C-plane.

Takashi Egawa (Nagoya) – Heteroepitaxial Growth of GaN-on-Si and Power Devices Applications (Plenary Talk)

GaN devices are promising for low-loss and high power applications. The conventional GaN-on-Si structures have the limitations of large lattice and thermal expansion-coefficient mismatches leading to high dislocation densities, wafer bowing and crack formations. To accommodate high breakdown voltage, thicker buffers are needed which suffers from much severe problems listed above. This talk presented a AlGaN/AlN super lattice (SL) buffer structure claiming to have less issues in wafer bowing and dislocations leading to a better breakdown with the increase of buffer thickness.

The AlGaN/AlN SL buffer structure firstly prevented the contact between Ga and Si which may form V-pits causing breakdown issues. Secondly, the conventional GaN buffer structure on Si substrate were claimed to have tensile stress, leading to wafer bowing and high density of defects, especially for thick buffers. The proposed SL structure, on the other hand, induced a compress stress which compensates the tensile stress induced by the top AlGaN/GaN layer, and therefore, resulted in an improve breakdown voltage. The author claimed a bowing free and cracks free SL structure with buffer layer thickness of 7 µm, which is a significant improvement compared to the conventional 7 µm thick buffer structures. The breakdown voltage of the proposed SL buffer structures with different buffer thickness were measured using normally-off GaN HEMTs based on the gate recessing and MOS technologies. The results showed a linear relationship between the thickness of the buffer and the breakdown voltage, which indicated a good quality of the buffer structure. EL technology was also used to examine the buffer quality, showing a uniform illuminance between the gate and drain for the devices on SL buffer structure which indicated a uniform field across the region and thus good buffer quality. On the other hand, only points of illuminance, which represented for the peak electric field, was observed for devices on the conventional buffer structure between the gate and drain due to defects and dislocations in the buffer.

Peter Brueckner (Fraunhofer) – High Frequency GaN HEMTs and MMICs with AlN-Interlayer (Oral Presentation)

AlGaN/GaN HEMTs with high saturation electron velocity and high 2DEG density have gained increasing attraction in RF technologies including high frequency MMICs for a variety of the applications. Advances in the scaling of the GaN devices have enabled a high f_T but the optimisation of the sheet resistance and the reduction of the parasitic components remain challenging. This talk presented a 100 nm AlGaN/GaN HEMT with AlN interlayer to reduce the sheet resistance, for low power E-band applications.

By using a AlN interlayer in the AlGaN/GaN structure, the Al-fraction in the barrier was effectively increased, and thus the sheet resistance was reduced. However, the formation of a good ohmic contact on the structure with high Al fraction became challenging. This talk used Si implantation on the ohmic contact regions to overcome this issue. Experimental results of the 100 nm devices showed ohmic contact resistance of 0.25 Ω*mm and sheet resistance of 300 Ω/sq, respectively. To reduce the parasitic components in the device especially the gate-drain capacitance, the passivation underneath the T-shape gate was carefully optimised. The parasitic capacitance was claimed to be reduced by tuning the dielectric constant around the gate. The fabricated 100 nm device exhibited an output current over 1 A/mm and a trans-conductance of 500 mS/mm. The breakdown voltage was over 40 V

and the cut off frequency was more than 100 GHz. The power density was as high as 1.9 W/mm at 94 GHz in continuous-wave load-pull operation.

Hiroji Kawai (Powdec) – Low-Cost High-Voltage GaN Lateral-Superjunction Power Transistors (Oral Presentation)

Conventional AlGaN/GaN HFETs are relying on field plates (FP) and conductive Si substrate to reduce the current collapse. In addition, there are still peak fields after the FP modulation between the gate and drain region. This results in a trade-off between the current collapse and the breakdown voltage of the GaN HFETs. This talk presented a polarization superjunction (PSJ) FETs fabricated on sapphire substrate and compared its performance and cost with the conventional GaN-on-Si devices.

The proposed PSJ structure was consist of a GaN/AlGaN/GaN trilayer and was induced between the gate and drain. Due to the high piezo-polarization and spontaneous polarization, a two 2DEG and a 2DHG were formed in the PSJ structure. With a reverse gate bias, the region underneath the PSJ was well depleted resulting in a high resistivity, and therefore a flat distribution of the electric field along the channel. This effectively enhanced the lateral breakdown as well as the dynamic R_{on}. The breakdown voltage was confirmed scalable with the length of the PSJ. For a 40 µm PSJ, the breakdown voltage was more than 6 kV. No dynamic R_{on} issue was observed for the device under 1047 V stress test.

The author also claimed that the cost of the PSJ FETs on sapphire substrate was less compared to the conventional GaN-on-Si HFETs. Firstly, to achieve a high breakdown voltage, a thick buffer layer of 5 µm or more was needed for the GaN/Si devices. This took longer time to grow compared to PSJ devices with 1 µm buffer thickness. In addition, the sapphire substrate was based on a LED compatible process and was also faster. Finally, the fabrication of the FPs on top of the GaN/Si based devices could also increase the total cost.

Yufei Wu (MIT) – Anomalous Source-Side Degradation of InAlN/GaN HEMTs under On-State Stress (Oral Presentation)

InAlN/GaN HEMTs have been emerged as promising candidates for high power millimetre wave applications due to the excellent gate length scaling. However, because of the high 2DEG density and very thin barrier thickness, there are a few reliability issues such as the high gate leakage current and V_{th} instability. This talk discussed the degradation mechanisms of the InAlN/GaN devices under on-state stresses.

The standard InAlN/GaN HEMTs fabricated on SiC substrate was stressed under +2 V gate voltage for 5 min with maximum drain current at room temperature. After that, an increase in the gate current (I_g) and source current (I_s) were observed and were larger than the drain current (I_d). This indicated that the degradation happens at the source. A temperature dependent measurement was then conducted on the devices with and without the on-state stress. The experimental results showed that before the on-state stress, thermo-emission was dominated in all I_g, I_s and I_d which were temperature dependent. However, after the on-state stress, I_g and I_s were no longer temperature dependent indicating a different mechanism (tunnelling like) while the I_d was still temperature dependent. Under high gate bias, the defect formation in the AlN barrier on the source side was concluded as the main reason for the increased gate leakage current. A symmetrical device structure was measured under the same condition showing the same degradation but on both source and drain side, which further proved the mechanism proposed in the talk.

Conclusion

I would like to thank UKNC for funding me for this conference (IWN2016). I was impressed by the quality of the papers and gained knowledge from all the presentations I attended, which covers a wide range of the GaN power and RF devices related topics, from solving the existing issues in the lateral devices (e.g. current collapse issues or the threshold voltage instability) to the development and design of several novel vertical structures. In addition, topics more towards application of the GaN device were also discussed, including the thermal management in GaN power devices and the integration of the GaN power module. I had a chance to have some discussion with the students from Rensselaer Polytechnic Institute, UCSB and Arizona State University, regarding to the switching performance of the p-AlGaN lateral device and their modified vertical CAVET structures. Attending this conference opens some new thoughts in my mind also, possibilities for a following project/proposal combining with what people are doing at present (in both vertical and lateral structures) with our current work.