ICNS-11 Conference Report William Waller HH Wills Physics Laboratory, Tyndall Avenue, Bristol, BS8 1TL. <u>Ww0206@bristol.ac.uk</u>

Introduction

The 11th International Conference on Nitride Semiconductors (ICNS-11) was held in Beijing China from 30 August - 4th September. The conference location was right outside the National Olympic Stadium known as The Bird's Nest. ICNS is a biannual conference and was chaired by Guoyi Zhang from Peking University, Akihiko Yoshikawa from Chiba University Bernard Gil from Univ. Montpellier II and Fernando Ponce from Arizona State University.

There were 6 plenary speakers, 57 invited speakers, 297 oral presentations and 491 posters.

Sessions were divided into four categories, growth, basic physics, optical devices and electrical devices. These were then split into 40 technical sessions including: UV Materials and Devices, Novel Growth, Quantum Dots, Normally-off HEMTs, ISBT and DBR, Doping & Defects, GaN on Si, Nano and Low-dimensional Structures, BN and Related Materials, Novel HEMTs. There were also rump sessions which allowed an open forum for discussion on either UV Light Emitting Devices, Next Generation of Light emitting Devices or A Roadmap of GaN power versus those of Si, SiC and others.

Plenary Talks

There were 6 plenary talks given by Nicolas Granjean from EPFL, Yusuke Mori from Osaka Univ., James Speck from UCSB, Yifeng Wu from Transphorm, and Nobel Prize Laureates Hiroshi Amano from Nagoya Univ., and Shuji Nakamura from UCSB.

Hiroshi Amano opened the conference with a talk entitled *Lighting the Earth by LEDs*, about his career and the progression and potential of GaN as a material for LEDs and HEMTs. He pioneered the now standard technique of growing a thin AIN wetting layer on sapphire substrates before growing GaN on top. This technique vastly reduced the dislocation density and allowed multilayer structures to be created, and hence functioning blue LEDs to be built.

Shuji Nakamura followed this with a talk entitled *Developments of InGaN-based Double Hetero-Structure High Brightness Blue LEDs and Future Lighting.* Shuji Nakamura built on work done by Amano into p-doping of GaN and designed a thermal annealing method for activating acceptors which could be used in mass production. This enabled him to create a blue LED while at the Nichia corporation, he is widely considered the inventor of the blue LED.

Selected papers

Kevin J Chen gave a talk entitled *Optoelectronic Devices on AlGaN/GaN HEMT Platform* this was interesting as he presented a Schottky-on-heterojunction LED realised upon a standard AlGaN/GaN heterostructure. This could be seamlessly integrated onto HEMT

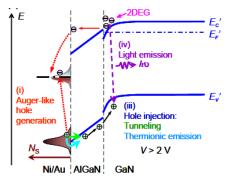


Figure 1: Illustration of Auger-like process of hole generation at forward biased Schottky junction. (K. Chen 2015)

technology. He described a process at the Schottky junction to explain the electron hole recombination required for the LED, this involved an Auger-like process which created the hole, see Fig. 1. The traditional Auger effect is where the energy of an electron falling to a lower energy state is absorbed by a different electron, ionising it from the atom. The talk was concluded with the claim that on chip hybrid opto-HEMTs could be used to minimise the impact of deep traps during dynamic operation of AlGaN/GaN power HEMTs. This was an interesting talk with good physics, however I feel that integrating an LED into the operation of a HEMT would likely lead to a drop in efficiency that would render it not useful for most applications.

Farid Medjdoub from IEMN – CNRS, France gave a talk entitled *Status and opportunities of ultrathin barrier GaN power devices*. In this talk I was particularly interested in a substrate removal technique for increasing breakdown voltage. Lateral GaN -on- Si devices were shown to have a breakdown path that went through the Si substrate. The technique provided local removal of the Si substrate under the HEMT device which increased the breakdown of devices from 750V to 1.9kV. This has been depicted in Fig. 2. The technique was described as fully scalable.

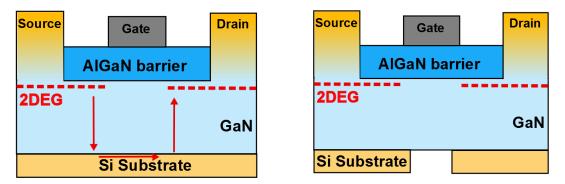


Figure 2: (left) Shows breakdown path through Si substrate. (right) Once the Si substrate is locally removed this breakdown path is eliminated greatly increasing the breakdown voltage of the device. (W. Waller 2015)

An entire session was dedicated to normally off HEMTs. Normally off HEMTs are desirable because they will act as a failsafe in high voltage applications. There are several methods to realise normally off, or enhancement mode, devices. These include a p-type epitaxy, fluorine plasma treatment and a recessed gate.

Three of the talks in this session used a recessed gate to achieve normally off operation. **Yuechan Kong** *et al.* deposited a HfO_2 layer by ALD after gate recess etching achieving a threshold voltage of 1.4V and current density of 834 mA/mm. **Ahmed Chakroun** *et al.* deposited a SiO_x layer by PECVDafter etching the gate with SF₆ based plasma. This showed a significant threshold voltage shift to -0.7V but did not render the device E-Mode. The maximum current density was 400mA/mm. **Bin Hou** *et al.* applied a multi-mesa-channel (MMC) technique in combination to flouring plasma treatment and a recessed gate. MMC devices have the gate wrap around the AlGaN layer. With this technology a V_{th} of 0.8V was achieved.

S. Jiang from the University of Sheffield presented a talk entitled *All GaN integrated cascade heterojunction field effect transistors*. This talk presented an integrated device which utilised a D-Mode and an E-Mode device. This mirrored the more common Si MOSFET cascade configuration. Using GaN integrated devices mitigated the Miller effect during switching leading to increased switching speed and reduced switching losses. The integration into one device provided a decrease in parasitic resistances. The E-Mode device was realised with fluoride ion implantation which moves the threshold to positive voltages.

These talks on E-Mode devices highlighted the difficulty in creating a normally off device without reducing channel mobility, on state carrier density or introducing additional trap levels. The challenge for the community and industrial partners in the near future will be creating an E-mode device that does not compromise significantly on performance.

I. C. Kizilyalli from Avogy inc. San Jose presented a talk entitled *Vertical power* semiconductor electronic devices based on bulk GaN substrates. Interest in developing GaN based power devices is increasing as the GaN figure of merit (FOM) is much better than Si. PN diodes, Schottky diodes and vertical transistors fabricated on psudo-bulk GaN substrates were presented. The PN devices demonstrated vertical breakdown voltages of more than 3700V with a differential specific on resistance of $3m\Omega cm^2$. Avalanche in GaN PN diodes was discussed. Vertical devices have the capability of achieving very high breakdown voltages, current breakdown voltages are limited by material quality as dislocations and defects create current paths through the device.

Posters

The poster sessions were split over two days. The first focussed upon growth and basic physics and the second upon electronic and optical devices. I particularly enjoyed the second poster session as it allowed me to meet students working on similar areas as myself, and engage is discussion about their work.

Naveen Karumuri presented a poster entitled *A Physics Based Current Compact model for GaN based HEMTs.* I thought this was interesting as I had done work on modelling HEMTs and was interested in how he modelled the mobility of the device, this is a parameter which will vary depending upon epitaxy and quality of the material. It will also vary with gate voltage. The model he presented was a good one for understanding the different effects in the AIGaN/GaN HEMT however it relied on a two parameter fit for the mobility as a function of gate potential. In my opinion these large degrees of freedom limit the usefulness of such a model.

Ankush Bag presented a poster entitled *Exploration into the Horizontal Tunneling of Drain Current of AlGaN/GaN HEMT on Sapphire: An insight to Interface Traps.* This poster described a jump in drain current at a particular Vd and Vg. The position of this jump was seen to have hysteric properties this is shown in Fig. 3. He attributed this jump to a Fowler-Nordheim tunnelling mechanism laterally through traps at the AlGaN/GaN interface. There was no attempt made to link the observed behaviour to this mechanism quantitatively. I felt that his conclusions were most likely misplaced, especially since this happened at a gate voltage where the device was not turned off (above threshold) and the dominant current is due to election drift through the channel. I think that this behaviour is most likely due to

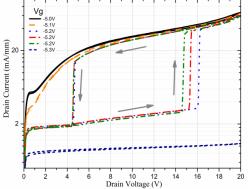


Figure 3: Observed jump in current observed by Ankush Bag *et al.* Huge increase in current was attributed to lateral Fowler-Nordheim tunnelling under the gated region. (A. Bag 2015)

device ringing – where stray capacitances and inductances due to unguarded measurement equipment cause the gate voltage to oscillate under particular conditions, thus changing the effective gate voltage. I suggested this idea to him and gave some ways that he might verify that this is not the case, for example shortening the cables to the measurement probes (thus changing the capacitance of the cables) and seeing if the conditions for the jump in current change. I also suggested changing the sweep rate.

Huarui Sun presented a poster entitled *GaN-on-Diamond for Ultra High Power Electronics*. This used a transient thermo-reflectance technique to measure the thermal conductivity of GaN on diamond wafers. GaN is grown on Si before the Si substrate is etched away, and then a thin layer of nano-crystalline diamond is deposited in its place using chemical vapour deposition. Diamond has a very high thermal conductivity allowing the device to operate at ultra-high power without reaching high temperatures which would be a reliability concern. In this work a laser rapidly heats a point on the wafer and the transient change in reflectance is measured in the nanoseconds after the heating, this corresponds to a temperature change. The short time required to measure a point allows the thermal conductivity to be mapped across the wafer.

Rump Session

I attended the rump session entitled *Roadmap of GaN power versus those of Si, SiC and others.* This turned out to be a lively session with some disagreement on the ability of GaN power electronics to overtake Si and SiC in the market. The session started with each member of the panel presenting a few slides detailing their opinion of the main obstacles for GaN and their roadmaps for overcoming them.

Tomas Palacios made an enthusiastic case for GaN overtaking Si and SiC for several power applications. The crux of his argument was that although currently SiC is better performing and Si is orders of magnitude cheaper, GaN possesses material properties such as higher mobility and higher breakdown voltage which will ultimately make it the preferred semiconductor for power applications. Crucially GaN benefits from an already mature multibillion dollar industry in LEDs, this means industry will always be improving growth methods and have the ability to create and improve GaN based power devices.

He also suggested that more work should be done on integrated circuits given the improved switching ability of GaN based systems. Other members of the panel were quick to point out the difficulty of creating logic with the lack of a good p-type GaN.

The problem referred to here is the one of Mg compensation. When GaN is doped with Mg, Mg will sit on the Ga site and act as an acceptor making the semiconductor p-type. However Mg is prone to form complexes, either with hydrogen or vacancies which compensate this effect, this makes it difficult to create a very strongly p-type GaN. Fig. 4 demonstrates this problem.

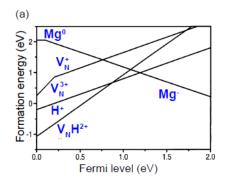


Figure 4: Formation energy of nitrogen vacancies decreases when the Fermi level is near the valence band. [1]

A different member of the panel was not so positive and emphasised the current cost of GaN based devices vs Si and how SiC is much further ahead than GaN, with devices already on the market. Once a technology has been adopted companies are reluctant to change direction due to the enormous cost associated with doing so.

One of the panel focussed upon alternative materials which could be competitive in the future for power electronics. He mentioned AIN and BN, but his main focus was on Ga_2O_3 . With a large bandgap of 4.8 eV, breakdown field of 8 MV/cm it is a contender for ultrahigh voltage power switching applications, in addition to this it can be grown via the same melt growth techniques used for sapphire substrates making it potentially much cheaper than its SiC and GaN competitors. Already 2-inch bulk wafers have been grown and MESFETs constructed [2].

Conclusions

Attending this conference was of great benefit to me as I was able to see a large range of results and I was in a position to talk to the authors of that work. I met a large number of researchers and gained knowledge and confidence in the field of III-Nitrides. I found the conference enthused me to jump back into my research with new fervour, it reminded me of the exciting field that I work in. I gained huge experience and confidence from presenting my work to a critical international audience and would like to thank UKNC for the financial support to help me achieve this.

References

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[2] M. Higashiwaki, *et al.,* "Development of gallium oxide power devices", *Phys. Status Solidi A*, vol. 211, no. 1, 2014.